# Intel® 31154 133MHz PCI Bridge

**Datasheet**

## Product Features

- PCI Bus Interfaces
- *PCI Local Bus Specification*, Revision 2.3 compliant
- *PCI-to-PCI Bridge Architecture Specification*, Revision 1.1 compliant
- *PCI Bus Power Management Interface Specification*, Revision 1.1 compliant
- *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a compliant
- Masquerade Mode
- Message Signal Interrupt (MSI) support
- External SROM support
- Vital Products Data (VPD) support
- Subsystem ID/Subsystem Vendor ID ECR support
- *Compact PCI Hot Swap Specification*, Revision 2.1 Support
- HW Support for Compact PCI (cPCI) Redundant System Slot configured platforms
- 64-bit Initiator/Target Capable
- 64-bit addressing
- Asynchronous cflocking in PCI mode
- Secondary Bus Arbitration
- Internal Arbiter Supports nine agents in addition to VerrazanoX
- Internal Arbitration can be disabled
- Optimized for PCI-X R1.0a mode
- Bus parking on bridge or last master
- Improved Buffer Architecture
- 8K Byte Data Buffers in each direction
- Improved level of Concurrency
- Up to nine outstanding transactions on each bus
- Scalability/Flexibility
- PCI R2.3 32/64-bit 33/66 MHz, 3.3 V
- 5 V Tolerant
- PCI-X R1.0a 32/64-bit 66/100/133 MHz, 3.3 V
- JTAG Interface
- GPIO Interface
- Allows simple software-controlled signaling protocols

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# Revision History

| Date | Revision | Description |
|---|---|---|
| May 2003 | 001 | Initial release |
| August 2003 | 002 | updated document title; corrected ballmap |
| January 2004 | 003 | updated Section 3.4 |

# Introduction 1

## 1.1 About This Document

This document provides information on the Intel® 31154 133MHz PCI Bridge, including a functional overview, mechanical data, package signal location and bus functional waveforms.

## 1.2 Product Overview

The Intel® 31154 133MHz PCI Bridge (also called 31154 Bridge) is a PCI component that functions as a highly concurrent, low latency transparent bridge between two PCI busses. The 31154 Bridge is capable of operating as a PCI-to-PCI bridge in the configurations shown in Table 1.

The 31154 Bridge is used on motherboards to provide additional I/O expansion slots. It is also used on PCI add-in cards as a means of mitigating the restrictive electrical loading constraints imposed on an expansion slot, enabling multiple conventional PCI or multiple PCI-X devices to reside on a single PCI I/O adapter.

The 31154 Bridge has additional hardware support for Compact PCI Hot Swap and Redundant System Slot via queue flush, arbiter lock, and clock output tri-stating.

The 31154 Bridge supports any combination of 32- and 64-bit data transfers on its primary and secondary bus interfaces. The bridge is 33/66 MHz capable in conventional PCI mode, and can run at 66 MHz, 100 MHz, or 133 MHz when operating in PCI-X mode depending upon its surrounding environment.

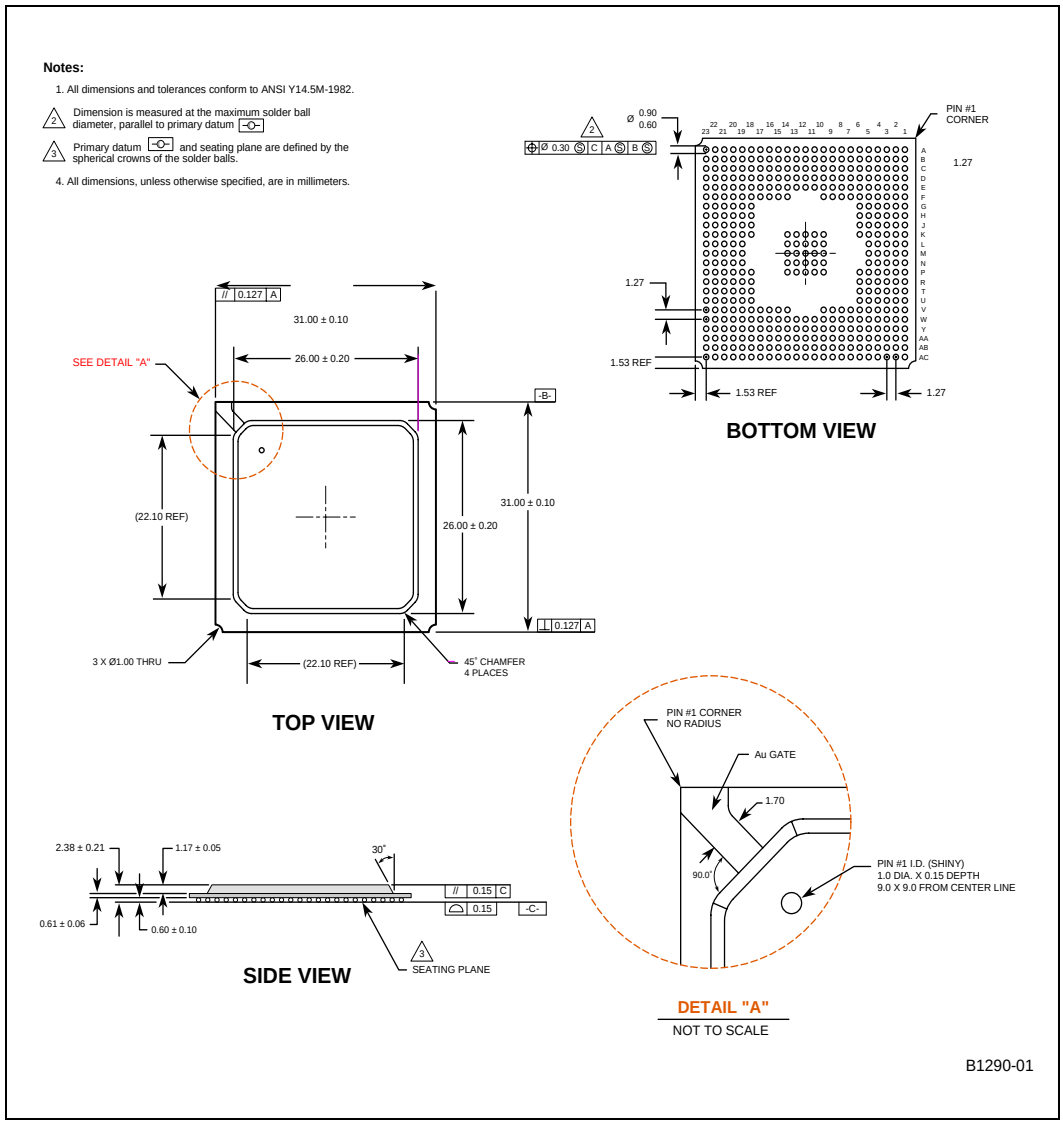
**Table 1. PCI to PCI Bridge Configurations**

| Primary Bus Interface | Secondary Bus Interface |
|---|---|
| PCI Local Bus Specification, Revision 2.3 | PCI Local Bus Specification, Revision 2.3 |
| PCI Local Bus Specification, Revision 2.3 | PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0b |
| PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0b | PCI Local Bus Specification, Revision 2.3 |
| PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0b | PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0b |

The 31154 Bridge is offered in a 421-lead PBGA package. This package is shown in Figure 1.

Figure 2 shows the left side of the 31154 Bridge ball map. Figure 3 shows the right side of the ball map.

## Figure 1. 31154 Bridge Assembly Drawing



## Figure 2. 31154 Bridge Ball Map – Left Side

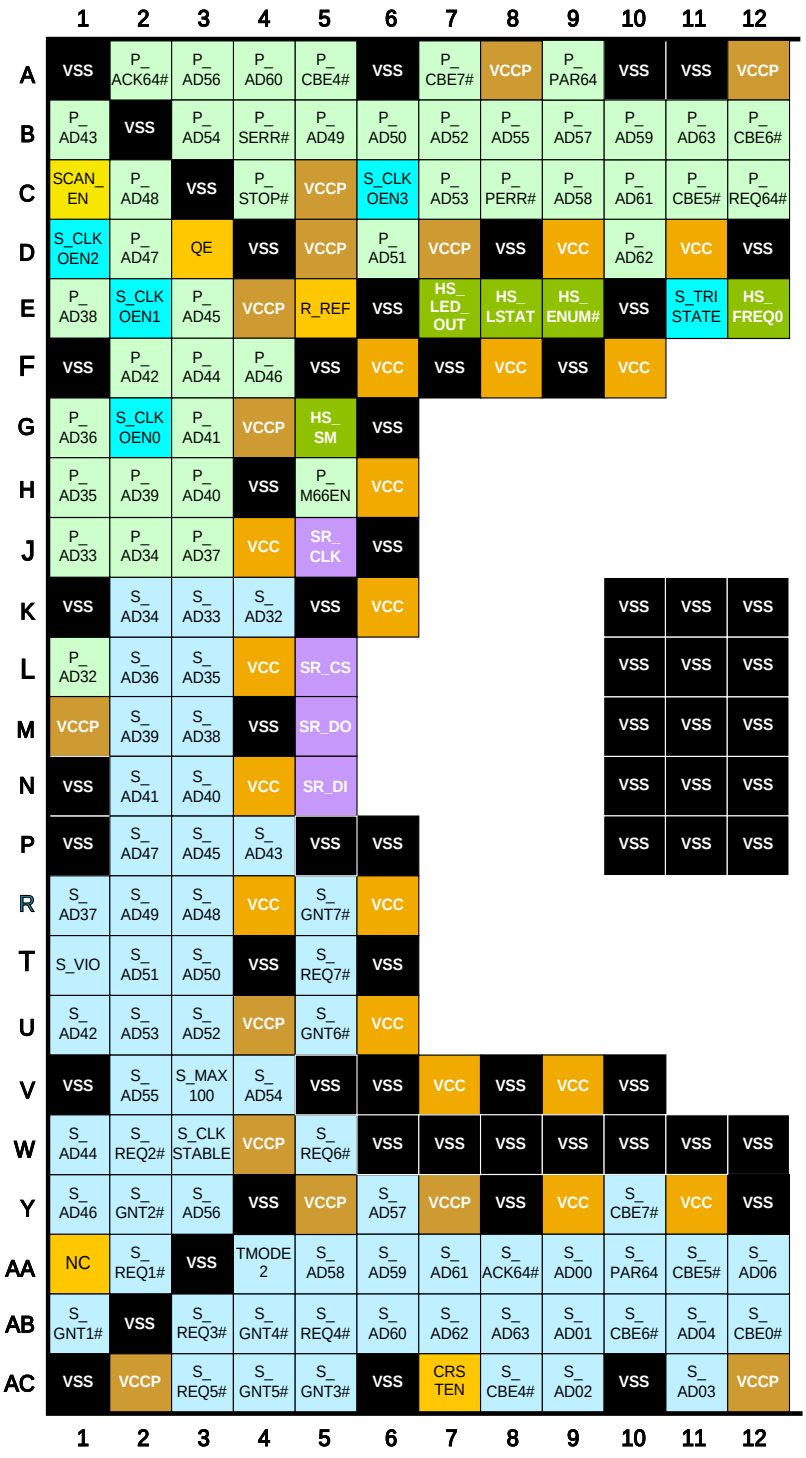
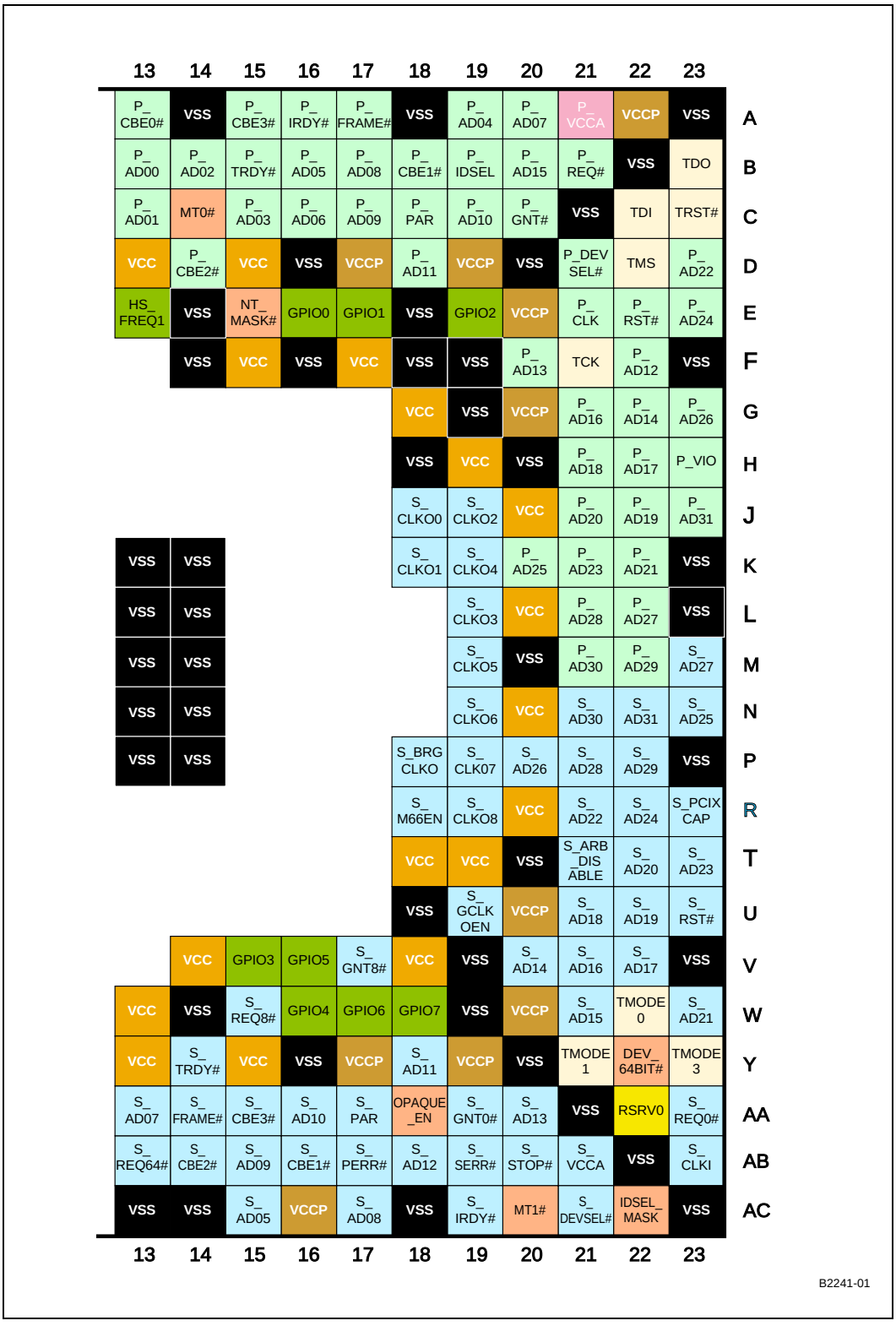


**Figure 3. 31154 Bridge Ball Map – Right Side**



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# Signal Pin Types and Descriptions 2

Table 2 lists and describes the 31154 133MHz PCI Bridge signal pin types.

**Table 2. Signal Pin Types**

| Symbol | Description |
|---|---|
| I | Input pin only |
| O | Output pin only |
| I/O | Pin can be either an input or output |
| OD | Open Drain pin |
| Ts | Tri-State |
| Sts | Sustained Tri-State |
| PWR | Power pin (See Section 2.9) |
| GND | Ground (See Section 2.9) |

The following sections describe the signals for the PCI interfaces.

- Section 2.1, “PCI Bus Interfaces”
- Section 2.2, “PCI Bus Interface 64-Bit Extension”
- Section 2.3, “Bus Interface Clocks and Reset”
- Section 2.4, “JTAG Interface”
- Section 2.5, “Serial EEROM Interface”
- Section 2.6, “Compact PCI Hot Swap Interface”
- Section 2.7, “Hardware Straps”
- Section 2.8, “Miscellaneous Signals”
- Section 2.9, “Power and Ground Signals”
- Section 2.10, “Ball Table Mappings”

The “#” symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name, the signal is asserted when at the high voltage level.

## 2.1 PCI Bus Interfaces

This section describes the signals related to the PCI Bus Interfaces. The 31154 133MHz PCI Bridge implements two independent PCI-X buses (a Primary and a Secondary bus). See the *PCI-X Addendum to the PCI Local Bus Specification 1.0b* for more information.

**Table 3. PCI Bus Interfaces (Sheet 1 of 3)**

| Signal | Width | Type | Description |
|---|---|---|---|
| P_AD[31:0]; S_AD[31:0] | 32; 32 | Ts-I/O | PCI Address/Data: These signals are a multiplexed address and data bus. During the address phase or phases of a transaction, the initiator drives a physical address on AD[31:0]. During the data phases of a transaction, the initiator drives write data, or the target drives read data. |
| P_CBE#[3:0]; S_CBE#[3:0] | 4; 4 | Ts-I/O | Bus Command and Byte Enables: These signals are a multiplexed command field and byte-enable field. During the address phase or phases of a transaction, the initiator drives the transaction type on C/BE#[3:0]. When there are two address phases, the first address phase carries the dual address command and the second address phase carries transaction type. For both read and write transactions, the initiator drives byte enables on C/BE#[3:0] during the data phases. |
| P_PAR; S_PAR | 1; 1 | Ts-I/O | Parity: Even parity calculated on 36 bits – AD[31:0] plus C/BE[3:0]#. This is calculated on all 36 bits regardless of the valid byte enables, and is generated for address and data phases. This is driven identically to the AD[31:0] lines, except that it is delayed by exactly one PCI clock. PAR is an output during the address phase for all 31154 133MHz PCI Bridge-initiated transactions and all data phases when 31154 133MHz PCI Bridge is the initiator of a PCI write transaction. |
| P_DEVSEL#; S_DEVSEL# | 1; 1 | Sts-I/ O | Device Select: As a target, the 31154 133MHz PCI Bridge asserts DEVSEL# when a PCI master peripheral attempts to access an internal address or the address of a resource that resides on the 31154 133MHz PCI Bridge's other bus. As an initiator, DEVSEL# indicates the response to a 31154 133MHz PCI Bridge-initiated transaction on the PCI bus. DEVSEL# is tri-stated from the leading edge of PCIRST#. DEVSEL# remains tri-stated by the 31154 133MHz PCI Bridge until driven as a target. |
| P_FRAME#; S_FRAME# | 1; 1 | Sts-I/ O | Frame: FRAME# is driven by the Initiator to indicate the beginning and duration of an access. While FRAME# is asserted, data transfers continue. When FRAME# is negated, the bus is either idle or is in the final data phase of the current bus transaction. |
| P_IRDY#; S_IRDY# | 1; 1 | Sts-I/ O | Initiator Ready: IRDY# indicates the ability of the initiator to complete the current data phase of the transaction. A data phase is completed when both IRDY# and TRDY# are sampled asserted. |
| P_TRDY#; S_TRDY# | 1; 1 | Sts-I/ O | Target Ready: Indicates the ability of the target to complete the current data phase of the transaction. A data phase is completed when both TRDY# and IRDY# are sampled asserted. TRDY# is tri-stated from the leading edge of PCIRST#. TRDY# remains tri-stated by the 31154 133MHz PCI Bridge until driven as a target. |
| P_STOP#; S_STOP# | 1; 1 | Sts-I/ O | Stop: Indicates that the target is requesting an initiator to stop the current transaction. |

## Table 3. PCI Bus Interfaces (Sheet 2 of 3)

| Signal | Width | Type | Description |
|---|---|---|---|
| P_PERR#;<br>S_PERR# | 1;<br>1 | Sts-I/ O | Parity Error:<br>Driven by an external PCI device when it receives data that has a parity error one PCI Clock following the PAR/PAR64 signal assertion. Driven by the 31154 133MHz PCI Bridge when, as an initiator, it detects a parity error during a read transaction as well as when receiving bad parity as the target of a write transaction. |
| P_SERR# | 1 | Od | Primary System Error:<br>SERR# can be pulsed active by any PCI device (including the 31154 133MHz PCI Bridge) that detects a system error. |
| S_SERR# | 1 | I | Secondary System Error:<br>SERR# can be pulsed active by any PCI device (except the 31154 133MHz PCI Bridge) that detects a system error condition. The 31154 133MHz PCI Bridge samples SERR# as an input and conditionally forwards it to its primary interface. |
| P_REQ# | 1 | Ts-O | Primary Bus Request:<br>The 31154 133MHz PCI Bridge bus acquisition request input to the primary bus arbiter. |
| P_GNT# | 1 | I | Primary Bus Grant:<br>Low assertion indicates that the 31154 133MHz PCI Bridge is granted primary bus ownership following the completion of the current primary bus transaction. |
| S_REQ[8:1]# | 8 | I | Secondary PCI Requests:<br>The internal arbiter supports up to nine external masters on the PCI bus using the S_REQ[8:1]# and S_REQ[0]# pins. |
| S_REQ[0]#/<br>BR_GNT# | 1 | I | Secondary PCI REQ[0]# or Bridge GNT#:<br>Depending upon whether or not the internal secondary arbiter is enabled, this signal serves as either a PCI request or a PCI grant.<br>• When secondary arbiter is enabled this input represents S_REQ[0]#.·<br>**When secondary arbiter is disabled, this input represents the 31154 133MHz PCI Bridge secondary bus master interface's PCI GNT#.** |
| S_GNT[8:1]# | 8 | Ts-O | Secondary PCI Grants<br>Supports up to nine other masters on the PCI bus. The arbiter can assert one of the nine bus grant outputs to indicate that an initiator can start a transaction on the PCI Bus following completion of the current transaction. |
| S_GNT[0]#/<br>BR_REQ# | 1 | TS-O | Secondary PCI GNT[0]# or Bridge REQ#:<br>Depending upon whether or not the internal secondary arbiter is enabled, this signal serves as either a PCI request or a PCI grant.<br>When secondary arbiter is enabled, this output represents S_GNT[0]#.<br>When secondary arbiter is disabled, this output represents the 31154 133MHz PCI Bridge secondary bus master interface's PCI REQ#. |

## Table 3. PCI Bus Interfaces (Sheet 3 of 3)

| Signal | Width | Type | Description |
|---|---|---|---|
| P_M66EN | 1 | I | Primary 66MHz Enable:<br>The Primary bus M66EN signal input is sampled on the trailing edge of P_RST#. This signal is used to determine the primary bus frequency when operating in conventional PCI mode.<br>When sampled as 1b, Indicates that the primary bus interface will be operating in 66MHz mode.<br>When sampled as 0b, Indicates that the 31154 133MHz PCI Bridge primary bus interface will be operating in 33MHz mode.<br>When the primary bus emerges from P_RST# in PCI-X mode, the PCI-X initialization pattern broadcast by the Originating Device (host bridge typically) determines the primary bus frequency. |
| P_IDSEL | 1 | I | Primary ID SEL:<br>This input serves as a high active chip select for Type 0 Configuration cycles that target the bridges configuration space registers. |
| S_M66EN | 1 | I | Secondary 66MHz Enable:<br>S_M66EN, along with S_PCIXCAP, indicate the mode (conventional PCI vs. PCI-X), and maximum frequency capabilities of the secondary bus devices. |
| S_PCIXCAP | 1 | I | Secondary PCI-X Capable:<br>S_PCIXCAP, along with S_M66EN, indicate the mode (conventional PCI vs. PCI-X), and maximum frequency capabilities of the secondary bus. ***Pin should be connected as shown in*** Table 4**.** |
| Total | 112 | | |

## Table 4. Device Mode/Frequency Capability Reporting

| M66EN | PCIXCAP | Convention PCI Device Frequency Capability | PCI-X Device Frequency Capability |
|---|---|---|---|
| Ground | Ground | 33 MHz | Not capable |
| Not connected | Ground | 66 MHz | Not capable |
| Ground | Pull-down | 33 MHz | PCI-X 66 MHz |
| Not connected | Pull-down | 66 MHz | PCI-X 66 MHz |
| Ground | Not connected | 33 MHz | PCI-X 133MHz |
| Not connected | Not connected | 66 MHz | PCI-X 133MHz |

## 2.2 PCI Bus Interface 64-Bit Extension

This section describes the signals related to 64 bit extension bus pins. Each PCI-X bus (Primary and Secondary) is capable of operating as a 32 or a 64 bit bus. Refer to PCI Local Bus Specification 3.0.

**Table 5. PCI Bus Interface 64-Bit Extension (Two Interfaces)**

| Signal | Width | Type | Description |
|---|---|---|---|
| P_AD[63::32] | 32 | Ts-I/O | PCI Address/Data:<br>Multiplexed upper address and data bus. This bus provides an additional 32 bits to the PCI bus. During the data phases of a transaction, the initiator drives the upper 32 bits of 64-bit write data, and during 64-bit read transactions the target drives the upper 32 bits of 64-bit read data. When not driven, AD[63:32] must be pulled up to a valid logic high level through external resistors. |
| S_AD[63::32] | 32 | | |
| P_CBE#[7::4] | 4 | Ts-I/O | Bus Command and Byte enables upper 4 bits:<br>These signals are a multiplexed command field and byte enable field. For both reads and write transactions, the initiator will drive byte enables for the AD[63:32] data bits on C/BE7:4] during the data phases when REQ64# and ACK64# are both asserted. When not driven, C/BE#[7:4] is pulled up to a valid logic high level through external resistors. |
| S_CBE#[7::4] | 4 | | |
| P_PAR64 | 1 | Ts-I/O | PCI interface upper 32-bits parity:<br>PAR64 carries the even parity of the 36 bits of AD[63:32] and C/BE#[7:4] for both address and data phases. When not driven, PAR64 is pulled up to a valid logic high level through an external resistor. |
| S_PAR64 | 1 | | |
| P_REQ64# | 1 | Sts-I/O | PCI interface request 64-bit transfer:<br>REQ64# is asserted by the initiator to indicate that the initiator is requesting a 64-bit data transfer. It has the same timing as FRAME#. When the 31154 133MHz PCI Bridge is the initiator, this signal is an output. When the 31154 133MHz PCI Bridge is the target, this signal is an input. |
| S_REQ64# | 1 | XX | XX |
| P_ACK64# | 1 | Sts-I/O | PCI interface acknowledge 64-bit transfer:<br>This is asserted by the target only when REQ64# is asserted by the initiator to indicate the target ability to transfer data using 64 bits. It has the same timing as DEVSEL#. |
| S_ACK64# | 1 | | |
| Total | 78 | | |

## 2.3 Bus Interface Clocks and Reset

Table 6 describes the signals related to bus interface clocks and reset.

**Table 6. Bus Interface Clocks and Reset**

| Signal | Width | Type | Description |
|---|---|---|---|
| P_CLK | 1 | I | Primary PCI Clock Input |
| S_BRGCLKO | 1 | O | Secondary Bridge Clock Output:<br>This output is identical to the other S_CLKO but does not have individual disable control. This signal is recommend, since the feedback clock for the bridge should be connected to S_CLKI when the internal clock generation is used. |
| S_CLKO[8::0] | 9 | O | Secondary PCI Clock Outputs:<br>33/66/100/133 MHz clock for secondary bus PCI devices. These clocks can be disabled by strapping the S_CLKOEN[3:0] pins during reset. |
| S_CLKI | 1 | I | Secondary PCI Clock In:<br>This signal is connected to an output of the low skew PCI clock buffer tree. When using the internal secondary clock generation, this pin should be connected to the S_BRGCLKO output. |
| S_CLKSTABLE | 1 | I | Secondary Clock Stable:<br>This input is used to enforce the $T_{rst-clk}$ time as defined in the PCI Local Bus Specification. After this signal is asserted, the bridge will wait 100µS before de-asserting the secondary PCI reset.<br>When using the internal secondary clock generation, this pin should be tied high. |
| S_GCLKOEN | 1 | I | Secondary Global Clock Output Enable:<br>This pin should be pulled high to enable the secondary clock outputs.<br>When de-asserted (0b), all secondary clock outputs (S_CLKO[8::0] and S_BRGCLKO) will asynchronously tri-state.<br>If an external clock source is used on the secondary interface, this signal should be pulled-low. |
| S_CLKOEN[3:0] | 4 | I (strap) | Secondary Clock Enable<br>These pins control the reset value of bits 8:0. The binary encoding on these pins indicates the number of secondary clock enabled. |

**Table 6. Bus Interface Clocks and Reset**

| Signal | Width | Type | Description |
|---|---|---|---|
| P_RST# | 1 | I | Primary PCI Reset |
| S_RST# | 1 | O | Secondary PCI Reset:<br>The 31154 133MHz PCI Bridge asserts S_RST# to reset devices that reside on its secondary PCI bus. The 31154 133MHz PCI Bridge asserts S_RST# due to one of the following events:<br>• P_RST# assertion·<br>• Setting the Secondary Bus Reset bit (bit 6) in the Bridge Control Register.<br>If PME# support from the $D3_{cold}$ is required, then a weak pull-down should be placed on the S_RST# line. This, in conjunction with PME# which is routed around the bridge, enables ACPI S3 (or higher) PME# operation for downstream PCI-PM compliant PCI agents. |
| Total | 20 | | |

## 2.4 JTAG Interface

Table 7 describes the signals related to the JTAG interface.

**Table 7. JTAG (Sheet 1 of 2)**

| Signal | Width | Type | Description |
|---|---|---|---|
| TDI | 1 | I | Test Data In:<br>TDI is the serial input through which JTAG instructions and test data enter the JTAG interface. TDI is sampled on the rising edge of TCK. If TDI is not driven, it produces the same results as if TDI were driven high. |
| TDO | 1 | O | Test Data Out:<br>TDO is the serial output through which test instructions and data from the test logic leave 31154 133MHz PCI Bridge. |
| TMS | 1 | I | Test Mode Select:<br>TMS causes state transitions in the test access port (TAP) controller. If TMS is not driven, it produces the same results as if TMS were driven high. |
| TCK | 1 | I | Test Clock:<br>TCK is the clock controlling the JTAG logic. For systems that do not implement JTAG, this input should be pulled low. |
| TRST# | 1 | I | Test Reset:<br>When TRST# is asserted (driven low), the TAP controller is asynchronously forced to enter a reset state, which in turn asynchronously initializes other test logic.<br>TRST# must be pulled low to GND for normal operation. |
| SCAN_EN | 1 | I | SCAN Mode Select:<br>The SCAN_EN pin toggles between the shift operation and the capture operation in the scan testing mode. It is used for scan chain testing of the device only. During normal operation, this input should be tied low. |

**Table 7. JTAG (Sheet 2 of 2)**

| Signal | Width | Type | Description |
|---|---|---|---|
| TMODE[3:0] | 4 | I | Test Mode Select:<br>These four pins are used to internally test 31154 133MHz PCI Bridge at the time of manufacture.<br>TMODE3 must be tied to $V_{SS}$ (logic 0) for normal operation.<br>TMODE[2:0] all three pins must be tied to VSS (preferred) or all must be tied to $V_{CC}$.<br>Normal Operation => 0000 or 0111. |
| MT#[1:0] | 2 | I | Manufacture Test pins.<br>These two pins must be pulled high for normal operation. |
| Total | 12 | | |

## 2.5 Serial EEROM Interface

Table 8 describes the signals related to the Serial EEROM interface.

**Table 8. Serial EEROM Interface**

| Signal | Width | Type | Description |
|---|---|---|---|
| SR_CLK | 1 | Ts-O | Serial EEROM Clock:<br>Clock output. This pin is connected to the EEROM clock input |
| SR_DI | 1 | Ts-O | Serial EEROM Data In:<br>Serial data stream output that is connected to the EEROM DI input. |
| SR_DO | 1 | I | Serial EEROM Data out:<br>Serial data stream input that is connected to the EEROMs DO output |
| SR_CS | 1 | Ts-O | Serial EEROM chip select:<br>The 31154 133MHz PCI Bridge drives this signal high to enable the serial ROM for a read or write cycle. |
| Total | 4 | | |

## 2.6 Compact PCI Hot Swap Interface

Table 9 describes the signals related to the cPCI PCS Hot Swap interface.

**Table 9. Compact PCI Hot Swap**

| Signal | Width | Type | Description |
|---|---|---|---|
| HS_ENUM# | 1 | Od-O | Primary Bus Compact PCI Hot Swap Event:<br>This is conditionally asserted to notify the system host that either a board has been freshly inserted or is about to be extracted. This signal informs the system host that the configuration of the system has changed. The system host then performs any necessary maintenance, such as installing or quiescing a device driver. |
| HS_LSTAT | 1 | I | Compact PCI Hot Swap Latch Status:<br>This is an input to the bridge, indicating the state of the ejector switch.<br>0= Indicates the ejector switch is closed<br>1=Indicates the ejector switch is open<br>If Compact PCI Hot Swap is not supported, this signal must be tied low. |
| HS_LED_OUT | 1 | O | LED Output:<br>The 31154 133MHz PCI Bridge outputs a logic one to illuminate the Hot Swap LED. |
| HS_SM | 1 | I | Hot swap Startup Mode:<br>This pin is sampled at the rising edge of P_RST#. If 0b, The 31154 133MHz PCI Bridge retries any Type 0 Configuration cycles addressed to it until its serial ROM preload has completed. If 1b, the 31154 133MHz PCI Bridge ignores (causes a master abort) any Type 0 configuration cycles addressed to it until its serial ROM preload has completed.<br>This pin should be tied low for non-Hot Swap systems. |
| HS_FREQ[1:0] | 2 | I | This pins are reserved for determining Primary Bus frequency and mode during a PCI-X hot swap event and are valid only when HS_SM = 1. The bus frequency and mode are described below:<br>00 => PCI Mode, 33 or 66 MHz. Use P_M66EN to determine frequency<br>01 => PCI-X Mode, 66 MHz<br>10 => PCI-X Mode, 100 MHz<br>11 => PCI-X Mode, 133 MHz<br>These pins should be tied low for non-Hot Swap systems. |
| Total | 6 | | |

## 2.7 Hardware Straps

Table 10 describes the signals related to the hardware straps. These are sampled during and on the trailing edge of P_RST# to set the mode of operation of the device.

### Table 10. Hardware Straps

| Signal | Width | Type | Description |
|---|---|---|---|
| S_ARB_DISABLE/ S_ARB_LOCK | 1 | I | Secondary Arbiter Disable / Arbiter Lock:<br>If sampled as 1b at the trailing edge of P_RST#, the internal secondary bus arbiter is disabled. In this event S_GNT#[0] is used for the bridge's secondary bus request output, and S_REQ#[0] is used for the bridge's secondary bus grant input.<br>If a logic low is sampled at the trailing edge of P_RST#, the bridge's internal secondary arbiter is enabled for use. This pin must have either a pull-up resistor to $V_{DD}$, or a pull down resistor to Vss. It must no be left floating.<br>If sampled as 1b after the trailing edge of P_RST#, the bridge's internal secondary bus arbiter will lock and only provide the grant to itself. |
| S_MAX100 | 1 | I (strap) | Secondary Bus Maximum Frequency:<br>This trap bits, sampled on the trailing edge of P_RST#, provides the 31154 133MHz PCI Bridge with necessary system specific secondary bus loading information that is required to correctly establish the maximum secondary bus clock frequency when operating in PCI-X mode.<br>When asserted the secondary bus frequency will be limited to a maximum of 100MHz.<br>This pin must have either pull-up resistors to $V_{DD}$, or pull down resistors to Vss. It must not be left floating. |
| OPAQUE_EN | 1 | I (strap) | Opaque Memory Space Enable:<br>If sampled high at the trailing edge of P_RST#, the 31154 133MHz PCI Bridge will set bit 11 in the "offset 46H:VCR2 – the 31154 133MHz PCI Bridge Control Register 2". This will enable the Opaque Memory Base/Limit registers. This establishes a private memory space for secondary bus usage, independent of the 31154 133MHz PCI Bridge downstream forwarding configuration. |
| IDSEL_MASK | 1 | I (strap) | IDSEL Masking Enable.<br>If sampled high at the trailing edge of P_RST#, the 31154 133MHz PCI Bridge will change the default value of the "Offset 5CH: Secondary IDSEL Select Register – SISR". This will hide devices 16-21 from the host. |
| DEV_64BIT# | 1 | I (strap) | This signal is sampled on the trailing edge of P_RST# and sets bit 16 int the PCI-X Bridge Status Register. This strap is to support system management software and does not change the behavior to the bridge. |
| Total | 5 | | |

## 2.8 Miscellaneous Signals

Table 11 describes the signals related to the special features of the 31154 133MHz PCI Bridge.

**Table 11. Miscellaneous Signals (Sheet 1 of 2)**

| Signal | Width | Type | Description |
|---|---|---|---|
| QE | 1 | O | Queues Empty:<br>This output indicates the state of the 31154 133MHz PCI Bridge internal request and data queues. When at a logic high level, this signal indicate that the 31154 133MHz PCI Bridge internal queues are completely empty.<br>This state of this output is valid only when the NT_MASK# pin is asserted. |
| NT_MASK# | 1 | I | New Transaction Mask:<br>When this pin is sampled asserted (logic low level), the 31154 133MHz PCI Bridge does not enqueue any new transactions, except PCI configuration cycles targeting its configuration registers. Transactions enqueued at the time that this signal is sampled asserted are allowed to complete normally. Applications could, for example, use this pin and the QE pin to implement external hardware that flushes the 31154 133MHz PCI Bridge request and data queues. |
| S_TRISTATE | 1 | I | Secondary Bus Tri-State Enable:<br>All Secondary bus outputs (except S_BRGCLKO) are asynchronously tri-stated when this signal is asserted(1b).<br>In cPCI systems this input can be used to support Redundant System Slot (RSS) implementations.<br>In non-RSS platforms, this pin should be tied directly to ground. |
| GPIO[7:0] | 8 | I/O | General Purpose I/O. |
| P_VIO | 1 | I | Primary Bus PCI Universal I/O Voltage Reference:<br>This signal must be tied to either 3.3V or 5V, corresponding to the signaling environment of the primary PCI bus as described in the PCI Local Bus Specification. When any device on the primary bus uses 5V signaling levels, the system must connect P_VIO to 5V. P_VIO is connected to 3.3V by the system only when all the devices on the primary bus use 3.3V signaling levels. |
| S_VIO | 1 | I | Secondary Bus PCI Universal I/O Voltage Reference:<br>This signal must be tied to either 3.3V or 5V, corresponding to the signaling environment of the secondary PCI bus as described in the PCI Local Bus Specification. When any device on the secondary bus uses 5V signaling levels, the system must connect S_VIO to 5V. S_VIO is connected to 3.3V by the system only when all the devices on the secondary bus use 3.3V signaling levels. |
| R_REF | 1 | I | R_REF:<br>This pin is connected to an external (board-level) precision pull-down resistor. The resistor is used as a reference for setting the I/O buffers output drive AC and DC parametrics, enabling the output buffers to meet the PCI/PCI-X parametric specifications. R=30Ω |
| NC | 1 | O | No Connect:<br>This output should be left floating. |

**Table 11. Miscellaneous Signals (Sheet 2 of 2)**

| Signal | Width | Type | Description |
|---|---|---|---|
| RSRV[1:0] | 2 | I | Reserved:<br>The reserved inputs should be pulled to a valid logic level. |
| Total | 17 | | |

## 2.9 Power and Ground Signals

Table 12 describes the power and ground-related signals.

**Table 12. Power and Ground Signals**

| Signal | Type | Description |
|---|---|---|
| S_VCCA | PWR | Secondary bus clock PLL Supply Voltage |
| P_VCCA | PWR | Primary bus clock PLL Supply Voltage |
| VCC | PWR | 1.3V Supply Voltage |
| VCCP | PWR | 3.3V Supply Voltage |
| P_VIO | PWR | Primary Reference Supply Voltage |
| S_VIO | PWR | Secondary Reference Supply Voltage |
| VSS | GND | Ground |

## 2.10 Ball Table Mappings

The pinout for the 31154 133MHz PCI Bridge PCI-X to PCI-X Bridge is described in the following tables. Table 13 lists the pinout entries in ballpad number order. Table 14 lists the entries alphabetically in signal order.

**Table 13. Pinout – Ballpad Number Order (Sheet 1 of 7)**

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| A1 | VSS | A13 | P_CBE0# |
| A2 | P_ACK64# | A14 | VSS |
| A3 | P_AD56 | A15 | P_CBE3# |
| A4 | P_AD60 | A16 | P_IRDY# |
| A5 | P_CBE4# | A17 | P_FRAME# |
| A6 | VSS | A18 | VSS |
| A7 | P_CBE7# | A19 | P_AD04 |
| A8 | VCCP | A20 | P_AD07 |
| A9 | P_PAR64 | A21 | P_VCCA |
| A10 | VSS | A22 | VCCP |
| A11 | VSS | A23 | VSS |
| A12 | VCCP | B1 | P_AD43 |

## Table 13. Pinout – Ballpad Number Order (Sheet 2 of 7)

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| B2 | VSS | C17 | P_AD09 |
| B3 | P_AD54 | C18 | P_PAR |
| B4 | P_SERR# | C19 | P_AD10 |
| B5 | P_AD49 | C20 | P_GNT# |
| B6 | P_AD50 | C21 | VSS |
| B7 | P_AD52 | C22 | TDI |
| B8 | P_AD55 | C23 | TRST# |
| B9 | P_AD57 | D1 | S_CLKOEN2 |
| B10 | P_AD59 | D2 | P_AD47 |
| B11 | P_AD63 | D3 | QE |
| B12 | P_CBE6# | D4 | VSS |
| B13 | P_AD00 | D5 | VCCP |
| B14 | P_AD02 | D6 | P_AD51 |
| B15 | P_TRDY# | D7 | VCCP |
| B16 | P_AD05 | D8 | VSS |
| B17 | P_AD08 | D9 | VCC |
| B18 | P_CBE1# | D10 | P_AD62 |
| B19 | P_IDSEL | D11 | VCC |
| B20 | P_AD15 | D12 | VSS |
| B21 | P_REQ# | D13 | VCC |
| B22 | VSS | D14 | P_CBE2# |
| B23 | TDO | D15 | VCC |
| C1 | SCAN_EN | D16 | VSS |
| C2 | P_AD48 | D17 | VCCP |
| C3 | VSS | D18 | P_AD11 |
| C4 | P_STOP# | D19 | VCCP |
| C5 | VCCP | D20 | VSS |
| C6 | S_CLKOEN3 | D21 | P_DEVSEL# |
| C7 | P_AD53 | D22 | TMS |
| C8 | P_PERR# | D23 | P_AD22 |
| C9 | P_AD58 | E1 | P_AD38 |
| C10 | P_AD61 | E2 | S_CLKOEN1 |
| C11 | P_CBE5# | E3 | P_AD45 |
| C12 | P_REQ64# | E4 | VCCP |
| C13 | P_AD01 | E5 | R_REF |
| C14 | MT0# | E6 | VSS |
| C15 | P_AD03 | E7 | HS_LED_OUT |
| C16 | P_AD06 | E8 | HS_LSTAT |

**Table 13. Pinout – Ballpad Number Order (Sheet 3 of 7)**

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| E9 | HS_ENUM# | F15 | VCC |
| E10 | VSS | F16 | VSS |
| E11 | S_TRISTATE | F17 | VCC |
| E12 | HS_FREQ0 | F18 | VSS |
| E13 | HS_FREQ1 | F19 | VSS |
| E14 | VSS | F20 | P_AD13 |
| E15 | NT_MASK# | F21 | TCK |
| E16 | GPIO0 | F22 | P_AD12 |
| E17 | GPIO1 | F23 | VSS |
| E18 | VSS | F1 | VSS |
| E19 | GPIO2 | F10 | VCC |
| E20 | VCCP | F14 | VSS |
| E21 | P_CLK | G1 | P_AD36 |
| E22 | P_RST# | G2 | S_CLKOEN0 |
| E23 | P_AD24 | G3 | P_AD41 |
| F1 | VSS | G4 | VCCP |
| F2 | P_AD42 | G5 | HS_SM |
| F3 | P_AD44 | G6 | VSS |
| F4 | P_AD46 | G18 | VCC |
| F5 | VSS | G19 | VSS |
| F6 | VCC | G20 | VCCP |
| F7 | VSS | G21 | P_AD16 |
| F8 | VCC | G22 | P_AD14 |
| F9 | VSS | G23 | P_AD26 |
| F10 | VCC | H1 | P_AD35 |
| F14 | VSS | H3 | P_AD40 |
| F15 | VCC | H4 | VSS |
| F16 | VSS | H5 | P_M66EN |
| F17 | VCC | H6 | VCC |
| F18 | VSS | H18 | VSS |
| F19 | VSS | H19 | VCC |
| F20 | P_AD13 | H2 | P_AD39 |
| F21 | TCK | H20 | VSS |
| F22 | P_AD12 | H21 | P_AD18 |
| F23 | VSS | H22 | P_AD17 |
| F1 | VSS | H23 | P_VIO |
| F10 | VCC | J1 | P_AD33 |
| F14 | VSS | J2 | P_AD34 |

## Table 13. Pinout – Ballpad Number Order (Sheet 4 of 7)

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| J3 | P_AD37 | L20 | VCC |
| J4 | VCC | L21 | P_AD28 |
| J5 | SR_CLK | L22 | P_AD27 |
| J6 | VSS | L23 | VSS |
| J18 | S_CLKO0 | M1 | VCCP |
| J19 | S_CLKO2 | M2 | S_AD39 |
| J20 | VCC | M3 | S_AD38 |
| J21 | P_AD20 | M4 | VSS |
| J22 | P_AD19 | M5 | SR_DO |
| J23 | P_AD31 | M10 | VSS |
| K1 | VSS | M11 | VSS |
| K2 | S_AD34 | M12 | VSS |
| K3 | S_AD33 | M13 | VSS |
| K4 | S_AD32 | M14 | VSS |
| K5 | VSS | M19 | S_CLKO5 |
| K6 | VCC | M20 | VSS |
| K10 | VSS | M21 | P_AD30 |
| K11 | VSS | M22 | P_AD29 |
| K12 | VSS | M23 | S_AD27 |
| K13 | VSS | N1 | VSS |
| K14 | VSS | N2 | S_AD41 |
| K18 | S_CLKO1 | N3 | S_AD40 |
| K19 | S_CLKO4 | N4 | VCC |
| K20 | P_AD25 | N5 | SR_DI |
| K21 | P_AD23 | N10 | VSS |
| K22 | P_AD21 | N11 | VSS |
| K23 | VSS | N12 | VSS |
| L1 | P_AD32 | N13 | VSS |
| L2 | S_AD36 | N14 | VSS |
| L3 | S_AD35 | N19 | S_CLKO6 |
| L4 | VCC | N20 | VCC |
| L5 | SR_CS | N21 | S_AD30 |
| L10 | VSS | N22 | S_AD31 |
| L11 | VSS | N23 | S_AD25 |
| L12 | VSS | P1 | VSS |
| L13 | VSS | P2 | S_AD47 |
| L14 | VSS | P3 | S_AD45 |
| L19 | S_CLKO3 | P4 | S_AD43 |

**Table 13. Pinout – Ballpad Number Order (Sheet 5 of 7)**

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| P5 | VSS | U2 | S_AD53 |
| P6 | VSS | U3 | S_AD52 |
| P10 | VSS | U4 | VCCP |
| P11 | VSS | U5 | S_GNT6# |
| P12 | VSS | U6 | VCC |
| P13 | VSS | U18 | VSS |
| P14 | VSS | U19 | S_GCLKOEN |
| P18 | S_BRGCLKO | U20 | VCCP |
| P19 | S_CLKO7 | U21 | S_AD18 |
| P20 | S_AD26 | U22 | S_AD19 |
| P21 | S_AD28 | U23 | S_RST# |
| P22 | S_AD29 | V1 | VSS |
| P23 | VSS | V2 | S_AD55 |
| R1 | S_AD37 | V3 | S_MAX100 |
| R2 | S_AD49 | V4 | S_AD54 |
| R3 | S_AD48 | V5 | VSS |
| R4 | VCC | V6 | VSS |
| R5 | S_GNT7# | V7 | VCC |
| R6 | VCC | V8 | VSS |
| R18 | S_M66EN | V9 | VCC |
| R19 | S_CLKO8 | V10 | VSS |
| R20 | VCC | V14 | VCC |
| R21 | S_AD22 | V15 | GPIO3 |
| R22 | S_AD24 | V16 | GPIO5 |
| R23 | S_PCIXCAP | V17 | S_GNT8# |
| T1 | S_VIO | V18 | VCC |
| T2 | S_AD51 | V19 | VSS |
| T3 | S_AD50 | V20 | S_AD14 |
| T4 | VSS | V21 | S_AD16 |
| T5 | S_REQ7# | V22 | S_AD17 |
| T6 | VSS | V23 | VSS |
| T18 | VCC | W1 | S_AD44 |
| T19 | VCC | W2 | S_REQ2# |
| T20 | VSS | W3 | S_CLKSTABLE |
| T21 | S_ARB_DISABLE | W4 | VCCP |
| T22 | S_AD20 | W5 | S_REQ6# |
| T23 | S_AD23 | W6 | VSS |
| U1 | S_AD42 | W7 | VSS |

## Table 13. Pinout – Ballpad Number Order (Sheet 6 of 7)

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| W8 | VSS | Y23 | TMODE3 |
| W9 | VSS | AA1 | NC |
| W10 | VSS | AA2 | S_REQ1# |
| W11 | VSS | AA3 | VSS |
| W12 | VSS | AA4 | TMODE2 |
| W13 | VCC | AA5 | S_AD58 |
| W14 | VSS | AA6 | S_AD59 |
| W15 | S_REQ8# | AA7 | S_AD61 |
| W16 | GPIO4 | AA8 | S_ACK64# |
| W17 | GPIO6 | AA9 | S_AD00 |
| W18 | GPIO7 | AA10 | S_PAR64 |
| W19 | VSS | AA11 | S_CBE5# |
| W20 | VCCP | AA12 | S_AD06 |
| W21 | S_AD15 | AA13 | S_AD07 |
| W22 | TMODE0 | AA14 | S_FRAME# |
| W23 | S_AD21 | AA15 | S_CBE3# |
| Y1 | S_AD46 | AA16 | S_AD10 |
| Y2 | S_GNT2# | AA17 | S_PAR |
| Y3 | S_AD56 | AA18 | OPAQUE_EN |
| Y4 | VSS | AA19 | S_GNT0# |
| Y5 | VCCP | AA20 | S_AD13 |
| Y6 | S_AD57 | AA21 | VSS |
| Y7 | VCCP | AA22 | RSRV0 |
| Y8 | VSS | AA23 | S_REQ0# |
| Y9 | VCC | AB1 | S_GNT1# |
| Y10 | S_CBE7# | AB2 | VSS |
| Y11 | VCC | AB3 | S_REQ3# |
| Y12 | VSS | AB4 | S_GNT4# |
| Y13 | VCC | AB5 | S_REQ4# |
| Y14 | S_TRDY# | AB6 | S_AD60 |
| Y15 | VCC | AB7 | S_AD62 |
| Y16 | VSS | AB8 | S_AD63 |
| Y17 | VCCP | AB9 | S_AD01 |
| Y18 | S_AD11 | AB10 | S_CBE6# |
| Y19 | VCCP | AB11 | S_AD04 |
| Y20 | VSS | AB12 | S_CBE0# |
| Y21 | TMODE1 | AB13 | S_REQ64# |
| Y22 | DEV_64BIT# | AB14 | S_CBE2# |

## Table 13. Pinout – Ballpad Number Order (Sheet 7 of 7)

| Ball Number | Signal | Ball Number | Signal |
|---|---|---|---|
| AB15 | S_AD09 | AC8 | S_CBE4# |
| AB16 | S_CBE1# | AC9 | S_AD02 |
| AB17 | S_PERR# | AC10 | VSS |
| AB18 | S_AD12 | AC11 | S_AD03 |
| AB19 | S_SERR# | AC12 | VCCP |
| AB20 | S_STOP# | AC13 | VSS |
| AB21 | S_VCCA | AC14 | VSS |
| AB22 | VSS | AC15 | S_AD05 |
| AB23 | S_CLKI | AC16 | VCCP |
| AC1 | VSS | AC17 | S_AD08 |
| AC2 | VCCP | AC18 | VSS |
| AC3 | S_REQ5# | AC19 | S_IRDY# |
| AC4 | S_GNT5# | AC20 | MT1# |
| AC5 | S_GNT3# | AC21 | S_DEVSEL# |
| AC6 | VSS | AC22 | IDSEL_MASK |
| AC7 | RSRV1 | AC23 | VSS |

See Table 14 on page 30 for a list of pinout entries in signal order.

Table 14 lists the 31154 133MHz PCI Bridge pinout entries alphabetically in signal order.

**Table 14. Pinout – Signal Order (Sheet 1 of 6)**

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| DEV_64BIT# | Y22 | P_AD16 | G21 |
| GPIO0 | E16 | P_AD17 | H22 |
| GPIO1 | E17 | P_AD18 | H21 |
| GPIO2 | E19 | P_AD19 | J22 |
| GPIO3 | V15 | P_AD20 | J21 |
| GPIO4 | W16 | P_AD21 | K22 |
| GPIO5 | V16 | P_AD22 | D23 |
| GPIO6 | W17 | P_AD23 | K21 |
| GPIO7 | W18 | P_AD24 | E23 |
| HS_ENUM# | E9 | P_AD25 | K20 |
| HS_FREQ0 | E12 | P_AD26 | G23 |
| HS_FREQ1 | E13 | P_AD27 | L22 |
| HS_LED_OUT | E7 | P_AD28 | L21 |
| HS_LSTAT | E8 | P_AD29 | M22 |
| HS_SM | G5 | P_AD30 | M21 |
| IDSEL_MASK | AC22 | P_AD31 | J23 |
| NC | AA1 | P_AD32 | L1 |
| NT_MASK# | E15 | P_AD33 | J1 |
| OPAQUE_EN | AA18 | P_AD34 | J2 |
| P_ACK64# | A2 | P_AD35 | H1 |
| P_AD00 | B13 | P_AD36 | G1 |
| P_AD01 | C13 | P_AD37 | J3 |
| P_AD02 | B14 | P_AD38 | E1 |
| P_AD03 | C15 | P_AD39 | H2 |
| P_AD04 | A19 | P_AD40 | H3 |
| P_AD05 | B16 | P_AD41 | G3 |
| P_AD06 | C16 | P_AD42 | F2 |
| P_AD07 | A20 | P_AD43 | B1 |
| P_AD08 | B17 | P_AD44 | F3 |
| P_AD09 | C17 | P_AD45 | E3 |
| P_AD10 | C19 | P_AD46 | F4 |
| P_AD11 | D18 | P_AD47 | D2 |
| P_AD12 | F22 | P_AD48 | C2 |
| P_AD13 | F20 | P_AD49 | B5 |
| P_AD14 | G22 | P_AD50 | B6 |
| P_AD15 | B20 | P_AD51 | D6 |

## Table 14. Pinout – Signal Order (Sheet 2 of 6)

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| P_AD52 | B7 | P_VIO | H23 |
| P_AD53 | C7 | QE | D3 |
| P_AD54 | B3 | R_REF | E5 |
| P_AD55 | B8 | RSRV0 | AA22 |
| P_AD56 | A3 | RSRV1 | AC7 |
| P_AD57 | B9 | S_ACK64# | AA8 |
| P_AD58 | C9 | S_AD00 | AA9 |
| P_AD59 | B10 | S_AD01 | AB9 |
| P_AD60 | A4 | S_AD02 | AC9 |
| P_AD61 | C10 | S_AD03 | AC11 |
| P_AD62 | D10 | S_AD04 | AB11 |
| P_AD63 | B11 | S_AD05 | AC15 |
| P_CBE0# | A13 | S_AD06 | AA12 |
| P_CBE1# | B18 | S_AD07 | AA13 |
| P_CBE2# | D14 | S_AD08 | AC17 |
| P_CBE3# | A15 | S_AD09 | AB15 |
| P_CBE4# | A5 | S_AD10 | AA16 |
| P_CBE5# | C11 | S_AD11 | Y18 |
| P_CBE6# | B12 | S_AD12 | AB18 |
| P_CBE7# | A7 | S_AD13 | AA20 |
| P_CLK | E21 | S_AD14 | V20 |
| P_DEVSEL# | D21 | S_AD15 | W21 |
| P_FRAME# | A17 | S_AD16 | V21 |
| P_GNT# | C20 | S_AD17 | V22 |
| P_IDSEL | B19 | S_AD18 | U21 |
| P_IRDY# | A16 | S_AD19 | U22 |
| MT0# | C14 | S_AD20 | T22 |
| P_M66EN | H5 | S_AD21 | W23 |
| P_PAR | C18 | S_AD22 | R21 |
| P_PAR64 | A9 | S_AD23 | T23 |
| P_PERR# | C8 | S_AD24 | R22 |
| P_REQ# | B21 | S_AD25 | N23 |
| P_REQ64# | C12 | S_AD26 | P20 |
| P_RST# | E22 | S_AD27 | M23 |
| P_SERR# | B4 | S_AD28 | P21 |
| P_STOP# | C4 | S_AD29 | P22 |
| P_TRDY# | B15 | S_AD30 | N21 |
| P_VCCA | A21 | S_AD31 | N22 |

## Table 14. Pinout – Signal Order (Sheet 3 of 6)

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| S_AD32 | K4 | S_CBE4# | AC8 |
| S_AD33 | K3 | S_CBE5# | AA11 |
| S_AD34 | K2 | S_CBE6# | AB10 |
| S_AD35 | L3 | S_CBE7# | Y10 |
| S_AD36 | L2 | S_CLKI | AB23 |
| S_AD37 | R1 | S_CLKO0 | J18 |
| S_AD38 | M3 | S_CLKO1 | K18 |
| S_AD39 | M2 | S_CLKO2 | J19 |
| S_AD40 | N3 | S_CLKO3 | L19 |
| S_AD41 | N2 | S_CLKO4 | K19 |
| S_AD42 | U1 | S_CLKO5 | M19 |
| S_AD43 | P4 | S_CLKO6 | N19 |
| S_AD44 | W1 | S_CLKO7 | P19 |
| S_AD45 | P3 | S_CLKO8 | R19 |
| S_AD46 | Y1 | S_CLKOEN0 | G2 |
| S_AD47 | P2 | S_CLKOEN1 | E2 |
| S_AD48 | R3 | S_CLKOEN2 | D1 |
| S_AD49 | R2 | S_CLKOEN3 | C6 |
| S_AD50 | T3 | S_CLKSTABLE | W3 |
| S_AD51 | T2 | S_DEVSEL# | AC21 |
| S_AD52 | U3 | S_FRAME# | AA14 |
| S_AD53 | U2 | S_GCLKOEN | U19 |
| S_AD54 | V4 | S_GNT0# | AA19 |
| S_AD55 | V2 | S_GNT1# | AB1 |
| S_AD56 | Y3 | S_GNT2# | Y2 |
| S_AD57 | Y6 | S_GNT3# | AC5 |
| S_AD58 | AA5 | S_GNT4# | AB4 |
| S_AD59 | AA6 | S_GNT5# | AC4 |
| S_AD60 | AB6 | S_GNT6# | U5 |
| S_AD61 | AA7 | S_GNT7# | R5 |
| S_AD62 | AB7 | S_GNT8# | V17 |
| S_AD63 | AB8 | S_IRDY# | AC19 |
| S_ARB_DISABLE | T21 | MT1# | AC20 |
| S_BRGCLKO | P18 | S_M66EN | R18 |
| S_CBE0# | AB12 | S_MAX100 | V3 |
| S_CBE1# | AB16 | S_PAR | AA17 |
| S_CBE2# | AB14 | S_PAR64 | AA10 |
| S_CBE3# | AA15 | S_PCIXCAP | R23 |

## Table 14. Pinout – Signal Order (Sheet 4 of 6)

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| S_PERR# | AB17 | VCC | F10 |
| S_REQ0# | AA23 | VCC | F15 |
| S_REQ1# | AA2 | VCC | F17 |
| S_REQ2# | W2 | VCC | G18 |
| S_REQ3# | AB3 | VCC | H6 |
| S_REQ4# | AB5 | VCC | H19 |
| S_REQ5# | AC3 | VCC | J4 |
| S_REQ6# | W5 | VCC | J20 |
| S_REQ64# | AB13 | VCC | K6 |
| S_REQ7# | T5 | VCC | L4 |
| S_REQ8# | W15 | VCC | L20 |
| S_RST# | U23 | VCC | N4 |
| S_SERR# | AB19 | VCC | N20 |
| S_STOP# | AB20 | VCC | R4 |
| S_TRDY# | Y14 | VCC | R20 |
| S_TRISTATE | E11 | VCC | R6 |
| S_VCCA | AB21 | VCC | T18 |
| S_VIO | T1 | VCC | T19 |
| SCAN_EN | C1 | VCC | U6 |
| SR_CLK | J5 | VCC | V7 |
| SR_CS | L5 | VCC | V9 |
| SR_DI | N5 | VCC | V14 |
| SR_DO | M5 | VCC | V18 |
| TCK | F21 | VCC | W13 |
| TDI | C22 | VCC | Y9 |
| TDO | B23 | VCC | Y11 |
| TMODE0 | W22 | VCC | Y13 |
| TMODE1 | Y21 | VCC | Y15 |
| TMODE2 | AA4 | VCCP | A8 |
| TMODE3 | Y23 | VCCP | A12 |
| TMS | D22 | VCCP | A22 |
| TRST# | C23 | VCCP | AC2 |
| VCC | D9 | VCCP | AC12 |
| VCC | D11 | VCCP | AC16 |
| VCC | D13 | VCCP | C5 |
| VCC | D15 | VCCP | D5 |
| VCC | F6 | VCCP | D7 |
| VCC | F8 | VCCP | D17 |

## Table 14. Pinout – Signal Order (Sheet 5 of 6)

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| VCCP | D19 | VSS | F14 |
| VCCP | E4 | VSS | F16 |
| VCCP | E20 | VSS | F18 |
| VCCP | G4 | VSS | F19 |
| VCCP | G20 | VSS | F23 |
| VCCP | M1 | VSS | G6 |
| VCCP | U4 | VSS | G19 |
| VCCP | U20 | VSS | H4 |
| VCCP | W4 | VSS | H18 |
| VCCP | W20 | VSS | H20 |
| VCCP | Y5 | VSS | J6 |
| VCCP | Y7 | VSS | K1 |
| VCCP | Y17 | VSS | K5 |
| VCCP | Y19 | VSS | K10 |
| VSS | A1 | VSS | K11 |
| VSS | A6 | VSS | K12 |
| VSS | A10 | VSS | K13 |
| VSS | A11 | VSS | K14 |
| VSS | A14 | VSS | K23 |
| VSS | A18 | VSS | L10 |
| VSS | A23 | VSS | L11 |
| VSS | B2 | VSS | L12 |
| VSS | B22 | VSS | L13 |
| VSS | C3 | VSS | L14 |
| VSS | C21 | VSS | L23 |
| VSS | D4 | VSS | M4 |
| VSS | D8 | VSS | M10 |
| VSS | D12 | VSS | M11 |
| VSS | D16 | VSS | M12 |
| VSS | D20 | VSS | M13 |
| VSS | E6 | VSS | M14 |
| VSS | E10 | VSS | M20 |
| VSS | E14 | VSS | N1 |
| VSS | E18 | VSS | N10 |
| VSS | F1 | VSS | N11 |
| VSS | F5 | VSS | N12 |
| VSS | F7 | VSS | N13 |
| VSS | F9 | VSS | N14 |

**Table 14. Pinout – Signal Order (Sheet 6 of 6)**

| Signal | Ball Number | Signal | Ball Number |
|---|---|---|---|
| VSS | P1 | VSS | W9 |
| VSS | P5 | VSS | W10 |
| VSS | P6 | VSS | W11 |
| VSS | P10 | VSS | W12 |
| VSS | P11 | VSS | W14 |
| VSS | P12 | VSS | W19 |
| VSS | P13 | VSS | Y4 |
| VSS | P14 | VSS | Y8 |
| VSS | P23 | VSS | Y12 |
| VSS | T20 | VSS | Y16 |
| VSS | T4 | VSS | Y20 |
| VSS | T6 | VSS | AA3 |
| VSS | U18 | VSS | AA21 |
| VSS | V1 | VSS | AB2 |
| VSS | V5 | VSS | AB22 |
| VSS | V6 | VSS | AC1 |
| VSS | V8 | VSS | AC6 |
| VSS | V10 | VSS | AC10 |
| VSS | V19 | VSS | AC13 |
| VSS | V23 | VSS | AC14 |
| VSS | W6 | VSS | AC18 |
| VSS | W7 | VSS | AC23 |
| VSS | W8 | | |

§ §

# Electrical Specifications 3

This chapter describes the electrical specifications for the 31154 133MHz PCI Bridge.

## 3.1 Absolute Maximum Ratings

This section provides the Absolute Maximum ratings for the 31154 133MHz PCI Bridge. Do not exceed the parameters listed in Table 15. Operations at the Absolute Maximum ratings are not guaranteed.

***Caution:*** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage.

**Table 15. Absolute Maximum Ratings**

| Parameter | Maximum Rating |
|---|---|
| Storage Temperature | -55°C to +125°C |
| Case Temperature Under Bias | 0°C to +70°C |
| Supply Voltage VCCP wrt. VSS | 0.5V to +4.1V |
| Supply Voltage S_VIO;P_VIO | 0.5 to 5.5V |
| Supply Voltage VCC wrt. VSS | 0.5V to +2.3V (Note 1) |
| Voltage on Any pin (non 5V tolerant) wrt. VSS | 0.5V to $V_{CC}P$ + 0.5V |
| Voltage on Any pin (5V tolerant) wrt. VSS | 0.5V to 5.5V |
| **NOTE:**<br>1 - 2.3V for fuse programming **only**. Normally 2.1V. | |

## 3.2 Operating Conditions

Table 16 shows minimum and maximum voltage, frequency, and temperature specifications for the 31154 133MHz PCI Bridge.

***Caution:*** Operation beyond the specified Operating Conditions is not recommended and extended exposure beyond the Operating Conditions may affect device reliability.

**Table 16. Operating Conditions**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| VCCP | 3.3V Supply Voltage | 3.0 | 3.6 | V | |
| P_VIO; S_VIO | Reference Supply Voltage | 3.0 | 5.25 | V | See Section 3.4 |
| VCC | 1.3V Supply Voltage | 1.235 | 1.365 | V | Note 2 |

**Table 16. Operating Conditions**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| S_VCCA | PLL Supply Voltage | 1.235 | 1.365 | V | |
| P_VCCA | PLL Supply Voltage | 1.235 | 1.365 | V | |
| $F_{P\_CLK}$ | Input Clock Frequency | 0 | 133 | MHz | Note 1 |
| $F_{s\_CLK}$ | Input Clock Frequency | 0 | 133 | MHz | Note 1 |
| $T_C$ | Case Temperature Under Bias | 0 | 70 | °C | |
| **NOTES:**<br>1- Any input clock frequency less then 25MHz use PLL in bypass mode, PLL output not guaranteed.<br>2- VCC is increased to 2.3V during fuse programming | | | | | |

## 3.3 Power Supply and Thermal Requirements

Table 17 shows the power supply and thermal requirements for the 31154 133MHz PCI Bridge.

**Table 17. Power Supply and Thermal Requirements**

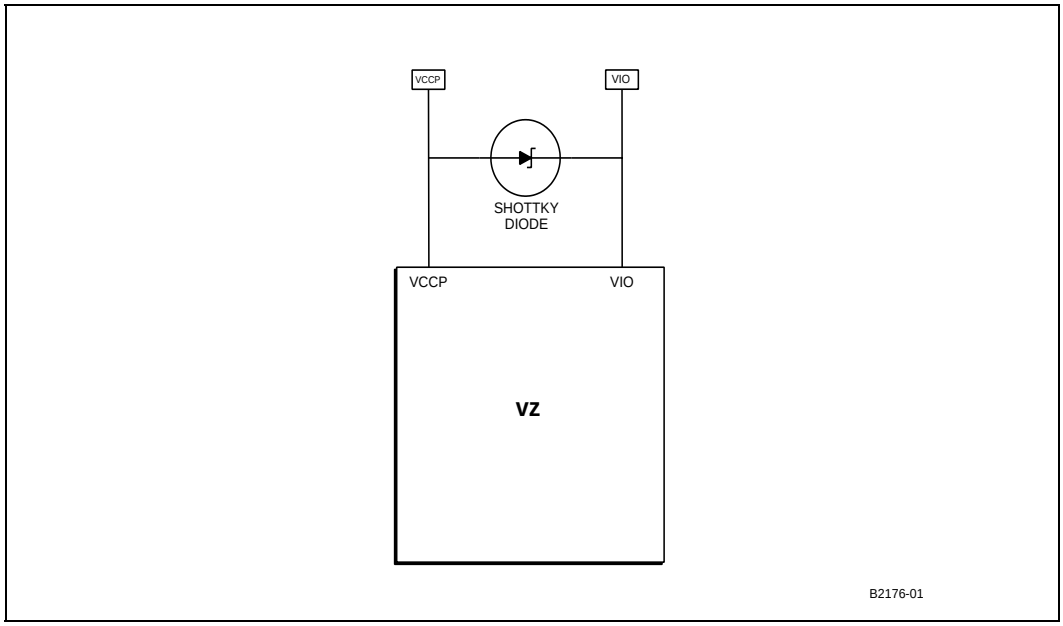
| Voltage | Typical | Maximum | Units | Notes |
|---|---|---|---|---|
| 3.3 V | | 2.5 | Watts | Note 1 |
| 1.3 V | | 0.70 | Watts | Note 1 |
| Operational (Thermal Power) | 1.75 | | Watts | Notes 2,3 |
| **NOTES:**<br>1- For Sizing 3.3V and 1.3V Supplies (instantaneous maximums)<br>2 - 3.3V and 1.3V in operational modes. For thermal calculations (sustained maximums).<br>3 -Tj=(80°C)+(1.75W)*(18.5°C/W) = 112°C | | | | |

## 3.4 Power Supply Special Considerations

If either P_VIO or S_VIO is not connected to the same power supply as Vccp, the user must perform one of the following steps:

- Ensure that the P_VIO or S_VIO power comes up before or simultaneously with Vccp and ensure that the P_VIO or S_VIO power goes down after or simultaneously with Vccp.
- Install a Shottky diode, as shown in Figure 4, between VCCP and the VIO pin/pins (as appropriate). The diode should be sized appropriately for the system's power environment. **(Recommended)**
- Connect a 25Ohm current limit resistor in series with the P_VIO and S_VIO supply. P_VIO and S_VIO can never be at a lower voltage than VCCP except in the case of a 25Ohm current limiting resistor in series with the P_VIO and S_VIO supply.

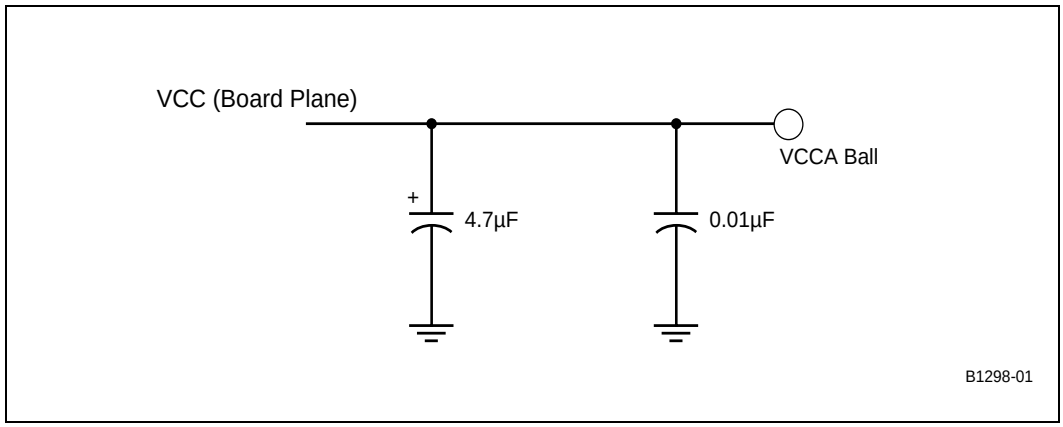
**Figure 4. Installing a Shottky Diode**




## 3.5 S_VCCA and P_VCCA Pin Requirements

To reduce clock skew and jitter, the P_VCCA and S_VCCA balls for the Phase Lock Loop (PLL) circuit are isolated on the package. The lowpass filter, as shown in Figure 5, reduces noise induced clock jitter and its effects on timing relationships in system designs. The 4.7 µF capacitor must be (low ESR solid tantalum), the 0.01 µF capacitor must be of the type X7R and the node connecting $V_{CCPLL}$ must be as short as possible. The $V_{SS}$ pins should be connected to the board ground plane immediately below capacitor.

**Figure 5. S_VCCA and P_VCCA Lowpass Filter**




# 3.6 Targeted DC Specifications

# 3.7 IO Types

Table 18 lists the 31154 133MHz PCI Bridge IO Types. These types are referred to in the subsections below.

**Table 18. IO Types**

| Name | Type |
|---|---|
| PCI | PCI only |
| PCIX | PCIX Only |
| PCI-X | Both PCI and PCIX |
| cmos | Non PCI-X compliant IO |

## 3.7.1 DC Characteristics

The DC characteristics for each pin include input sense levels and output drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. The DC Operating Conditions for the High- and Low-Strength Input, Output, and I/O pins are shown in Table 19.

**Table 19. DC Characteristics (Sheet 1 of 2)**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{IL1}$ | Input Low Voltage (cmos) | -0.3 | 0.8 | V | Note 2 |
| $V_{IH1}$ | Input High Voltage (cmos) | 2.0 | VCCP + 0.3 | V | |
| $V_{IL2}$ | Input Low Voltage (PCI-X) | -0.5 | 0.35VCCP | V | |
| $V_{IH2}$ | Input High Voltage (PCI-X/ PCI) | 0.5VCCP | VCCP + 0.5 | V | Note 1 |

**Table 19. DC Characteristics (Sheet 2 of 2)**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{IL3}$ | Input Low Voltage (PCI) | -0.5 | 0.3VCCP | V | |
| $V_{OL1}$ | Output Low Voltage (Misc) | | 0.4 | V | $I_{OL}$ = 4 mA |
| $V_{OH1}$ | Output High Voltage (Misc) | 2.4 | | V | $I_{OH}$ = -2 mA |
| $V_{OL3}$ | Output Low Voltage (PCI-X) | | 0.1VCCP | V | $I_{OL}$ = 1500uA (Note 1) |
| $V_{OH3}$ | Output HIGH Voltage (PCI-X) | 0.9VCCP | | V | $I_{OH}$ = -500uA (Note 1) |
| $C_{IN}$ | Input pin Capacitance | | 8 | pF | |
| $C_{CLK}$ | Clock pin Capacitance | 5 | 8 | pF | |
| $L_{PIN}$ | Pin Inductance | | 15 | nH | |
| **NOTES:**<br>1 - Pads are 5V Tolerant (not operational).<br>2 - CMOS IOs include all IOs that are not PCI or PCIX-compliant IOs. | | | | | |

## 3.7.2 $I_{cc}$ Characteristics

Table 20 describes the $I_{CC}$ characteristics.

**Table 20. Icc Characteristics (Sheet 1 of 2)**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $I_{LI1}$ | Input Leakage Current for each signal except TCK, TMS, TRST#, TDI | 140 | 1000 | µA | |
| $I_{LI2}$ | Input Leakage Current for TCK, TMS, TRST#, TDI | 140 | 1000 | µA | |
| $I_{CC33}$ Active (Power Supply) | Power Supply Current | | 0.70 | A | |
| $I_{CC13}$ Active (Power Supply) | Power Supply Current | | 0.65 | A | |
| $I_{CC13}$ Fuse Program (Power Supply) | Power Supply Current | .1 | .1 | A | |

**Table 20. Icc Characteristics (Sheet 2 of 2)**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $I_{CC33}$ Active (Power Modes) | Reset Mode<br>Hi-Z Mode | 0.1 | 0.2 | A | |
| $I_{CC13}$ Active (Power Modes) | Reset Mode<br>Hi-Z Mode | 0.5 | 0.70 | A | |
| $I_{CC}$ Active (Power Supply) value is provided for selecting your system's power supply. This is measured using one of the worst case instruction mixes with VCCP = 3.6V, VCC = 1.365V, and ambient temperature = 55 °C.<br><br>Input leakage currents include hi-Z output leakage for all bi-directional buffers with tri-state outputs. | | | | | |

# 3.8 Targeted AC Specifications

The AC characteristics for each pin are described in the following sections.

## 3.8.1 Input Clock Timings

This section describes PCI input clock timings for the 31154 133MHz PCI Bridge. Table 21 summarizes the minimum and maximum clock timings at 133, 100, 66, and 33 MHz.

**Table 21. Input Clock Timings**

| Symbol | Parameter | PCI-X 133 | | PCI-X 100 | | PCI-X 66 | | PCI 66 | | PCI 33 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $T_{F1}$ | PCI clock Frequency | 100 | 133 | 66 | 100 | 50 | 66 | 33 | 66 | 25 | 33 | MHz | Note 1 |
| $T_{C1}$ | PCI clock Cycle Time | 7.5 | 10 | 10 | 15 | 15 | 20 | 15 | 30 | 30 | 60 | ns | |
| $T_{CH1}$ | PCI clock High Time | 3 | | 3 | | 6 | | 6 | | 11 | | ns | |
| TCL1 | PCI clock Low Time | 3 | | 3 | | 6 | | 6 | | 11 | | ns | |
| TSR1 | PCI clock Slew Rate | 1.5 | 4 | 1.5 | 4 | 1.5 | 4 | 1.5 | 4 | 1 | 4 | V/ns | Note 2 |
| **NOTES:**<br>1- In PCI-33 clock can vary down to DC. Any input below 25MHZ must be in PLL bypass mode.<br>2 -This slew rate as defined in PCI, PCIX specifications<br>The minimum clock period must not be violated for any single clock cycle, i.e., accounting for all system jitter. | | | | | | | | | | | | | |

## 3.8.2 PCI Interface Signal Timings

This section shows the PCI interface signal timings for the 31154 133MHz PCI Bridge. Table 22 summarizes the minimum and maximum signal timings at 133, 100, 66, and 33 MHz.

## Table 22. PCI Signal Timings (Sheet 1 of 2)

| Symbol | Parameter | PCI-X 133 PCI-X 100 | | PCI-X 66 | | PCI 66 | | PCI 33 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $T_{OV1}$ | Clock to Output Valid Delay for bused signals | 0.7 | 3.8 | 0.7 | 3.8 | 1 | 6 | 2 | 11 | ns | Notes 1,2,6,7 |
| $T_{OV2}$ | Clock to Output Valid Delay for point to point signals | 0.7 | 3.8 | 0.7 | 3.8 | 2 | 6 | 2 | 12 | ns | Notes 1,2,6,7 |
| TOF | Clock to Output Float Delay | | 7 | | 7 | | 14 | | 28 | ns | |
| TIS1 | Input Setup to clock for bused signals | 1.2 | | 1.7 | | 3 | | 7 | | ns | Notes 1,3 |
| TIS2 | Input Setup to clock for point to point signals | 1.2 | | 1.7 | | 5 | | 10, 12 | | ns | Notes 1,3 |
| $T_{IH1}$ | Input Hold time from clock | 0.5 | | 0.5 | | 0 | | 0 | | ns | Notes 1,3 |
| $T_{RST}$ | Reset Active Time | 1 | | 1 | | 1 | | 1 | | ms | |
| $T_{RF}$ | Reset Active to output float delay | | 40 | | 40 | | 40 | | 40 | ns | |
| $T_{IS3}$ | REQ64# to Reset setup time | 10 | | 10 | | 10 | | 10 | | clocks | Notes 1,3 |
| $T_{IH2}$ | Reset to REQ64# hold time | 0 | 50 | 0 | 50 | 0 | 50 | 0 | 50 | ns | Notes 1,3 |
| $T_{IS4}$ | PCI-X initialization pattern to Reset setup time | 10 | | 10 | | | | | | clocks | 1,3 |

**Table 22. PCI Signal Timings (Sheet 2 of 2)**

| Symbol | Parameter | PCI-X 133 PCI-X 100 | | PCI-X 66 | | PCI 66 | | PCI 33 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| $T_{IH3}$ | Reset to PCI-X initialization pattern hold time | 0 | 50 | 0 | 50 | | | | | ns | 1,3 |

**NOTES:**
1 - See Figure 6
2 - See Figure 7
3 - See Figure 8
4 - See Table 27
5 - See Figure 9
6 - See Figure 10
7 - See Figure 11
8 - See Figure 12

## 3.8.3 PCI-X Slew Rates

Table 23 shows the PCI-X slew rates for the 31154 133MHz PCI Bridge.

**Table 23. PCI-X Slew Rates**

| Symbol | Parameter | Condition | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_r$ | Output rise slew rate | 0.3Vccp to 0.6Vccp | 1 | 4 | V/ns | Note 1 |
| $t_f$ | Output fall slew rate | 0.6Vccp to 0.3Vccp | 1 | 4 | V/ns | Note 1 |

**NOTE:**
1 – See Figure 12

## 3.8.4 Boundary Scan Test Signal Timings

Table 24 shows the boundary scan test signal timings for the 31154 133MHz PCI Bridge.

**Table 24. Boundary Scan Signal Timings (Sheet 1 of 2)**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| TBSF | TCK Frequency | 0 | 66 | MHz |
| $T_{BSCH}$ | TCK High Time | 7.5 | | ns |
| TBSCL | TCK Low Time | 7.5 | | ns |
| $T_{BSCR}$ | TCK Rise Time | | 5 | ns |
| $T_{BSCF}$ | TCK Fall Time | | 5 | ns |
| $T_{BSIS1}$ | Input Setup to TCK | 3 | | ns |
| $T_{BSIH1}$ | Input Hold from TCK | 3 | | ns |
| $T_{BSOV1}$ | TDO Output Valid Delay from falling edge of TCK. | 1 | 11 | ns |

**Table 24. Boundary Scan Signal Timings (Sheet 2 of 2)**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{OF1}$ | TDO Output Float Delay from falling edge of TCK. | 1 | 11 | ns |
| | TCK insertion delay. | 1.0 | 3.2 | ns |
| | Boundary Scan clock insertion delay. | 1.6 | 4.8 | ns |

## 3.8.5 CMOS General Purpose Interface Timings

Table 25 describes the CMOS general purpose signal timings.

**Table 25. CMOS General Purpose Interface Timings**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Tov | Output Delay Through Pad | 0.8 | 3.25 | nsec | Note 1 |
| $T_{OF}$ | Output Float Delay | 1.0 | 3 | nsec | Note 1 |
| $T_{IS}$ | Input Delay Through Pad | 0.8 | 2.0 | nsec | |
| $T_{IH}$ | Input Delay Through Pad | 0.8 | 2.0 | nsec | |
| **NOTES:**<br>1 – min load 10pf<br>2 – max load 40pf<br>See Figure 7. | | | | | |

## 3.8.6 Bypass Mode Timings

Table 26 describes the bypass mode timings.

**Table 26. Bypass Mode Timings**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| TOV | Output Valid Delay. Delay normal timings by 3.3ns. | | 3.3 | ns | 1 |
| 1 – The bypass clock insertion + delay at the slow corner is about 3.3nS. | | | | | |

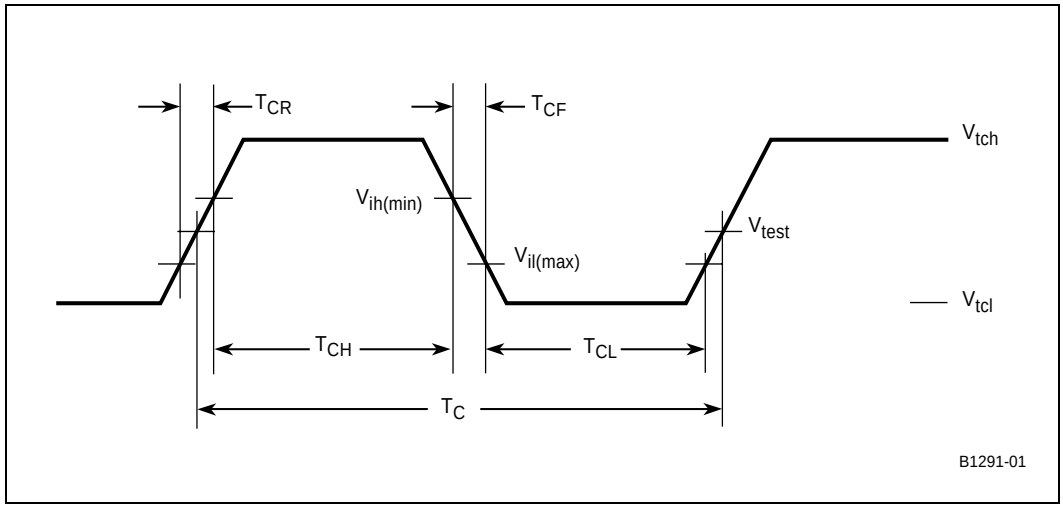
## 3.9 AC Timing Waveforms

The AC timing waveforms are described in the following sections.

### 3.9.1 Clock Timing Measurement Waveforms

Figure 6 illustrates the clock timing measurement waveforms.

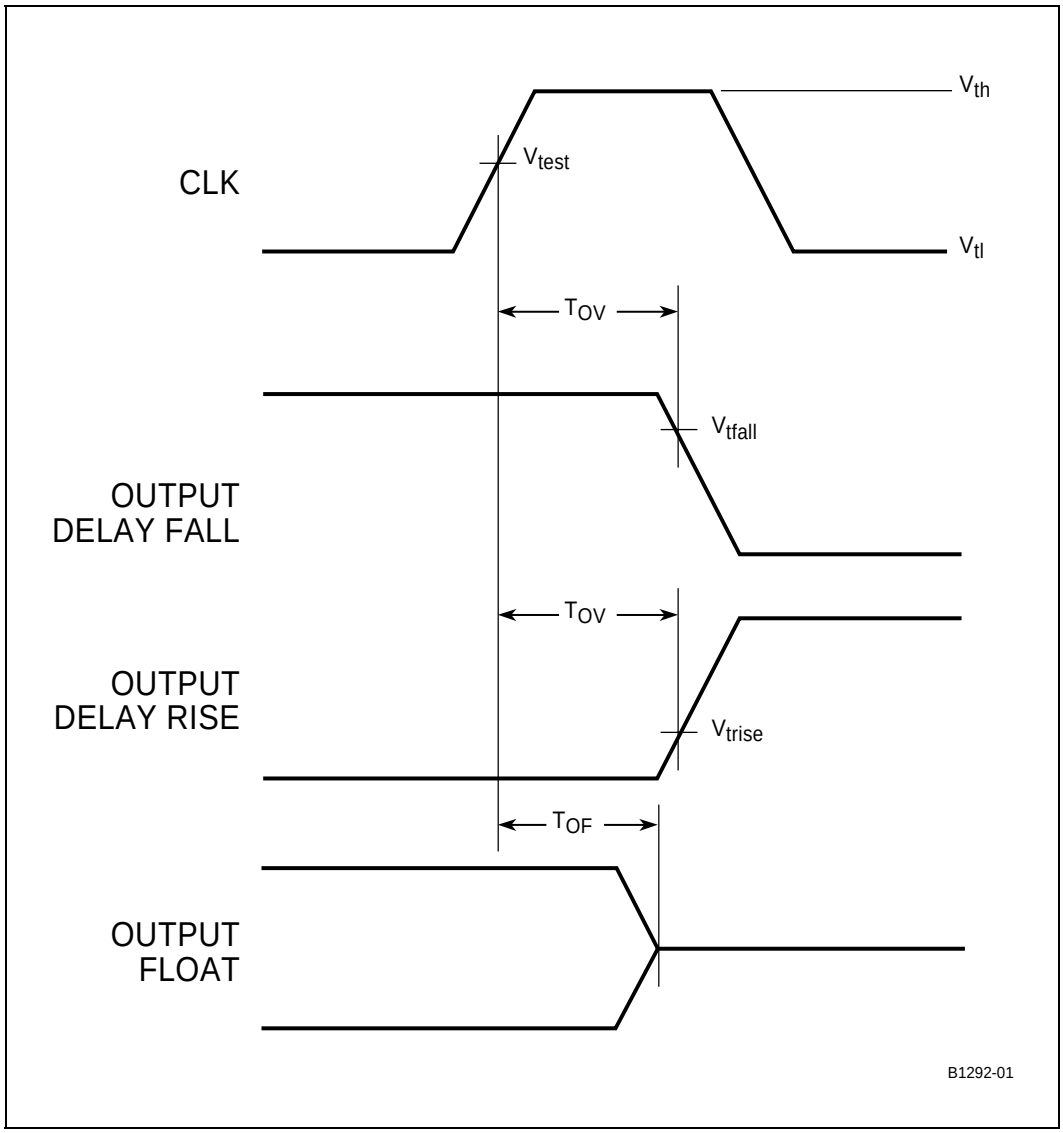
**Figure 6. Clock Timing Measurement Waveforms**



## 3.9.2 Output Timing Measurement Waveforms

Figure 7 illustrates the output timing measurement waveforms.

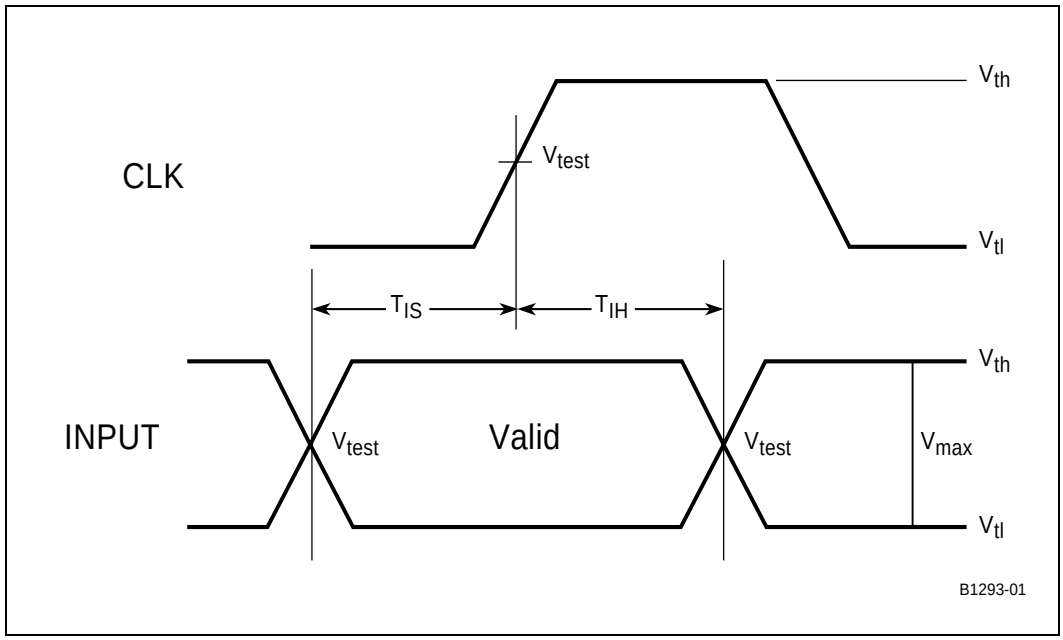
**Figure 7. Output Timing Measurement Waveforms**



### 3.9.3 Input Timing Measurement Waveforms

Figure 8 illustrates the input timing measurement waveforms.

**Figure 8. Input Timing Measurement Waveforms**




## 3.10 AC Test Conditions

Table 27 lists the AC test loads that are illustrated in the following sections.

**Table 27. AC Measurement Conditions**

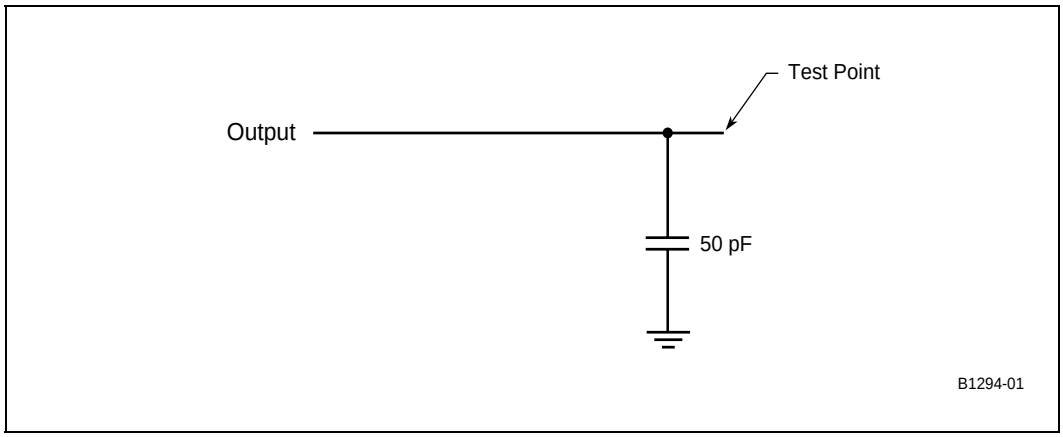
| Symbol | PCI-X | PCI | General IO | Units | Notes |
|---|---|---|---|---|---|
| Vth | 0.6VCCP | 0.6VCCP | 0.6VCCP | V | |
| $V_{tl}$ | 0.25VCCP | 0.2VCCP | 0.25VCCP | V | |
| Vtest | 0.4VCCP | 0.4VCCP | 0.4VCCP | V | |
| $V_{trise}$ | 0.285VCCP | 0.285VCCP | 0.285VCCP | V | |
| Vtfall | 0.615VCCP | 0.615VCCP | 0.615VCCP | V | |
| $V_{max}$ | 0.4VCCP | 0.4VCCP | 0.4VCCP | V | |
| Slew Rate | 1.5 | 1.5 | 1.5 | V/nS | Note 1 |

**NOTE:**
1 – Input signal slew rate is measured between Vil and Vih

### 3.10.1 AC Test Load for All Signals Except PCI-X

Figure 9. illustrates the AC test load for all signals **except** PCI-X.

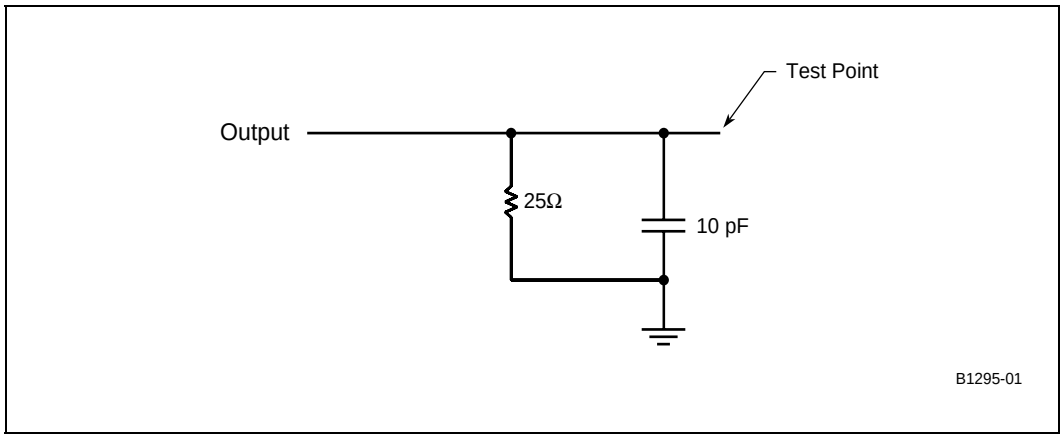
**Figure 9. AC Test Load for All Signals Except PCIX**




### 3.10.2 PCI/PCI-X $T_{ov(max)}$ Rising Edge AC Test Load

Figure 10 illustrates the PCI/PCI-X Rising Edge AC test load.

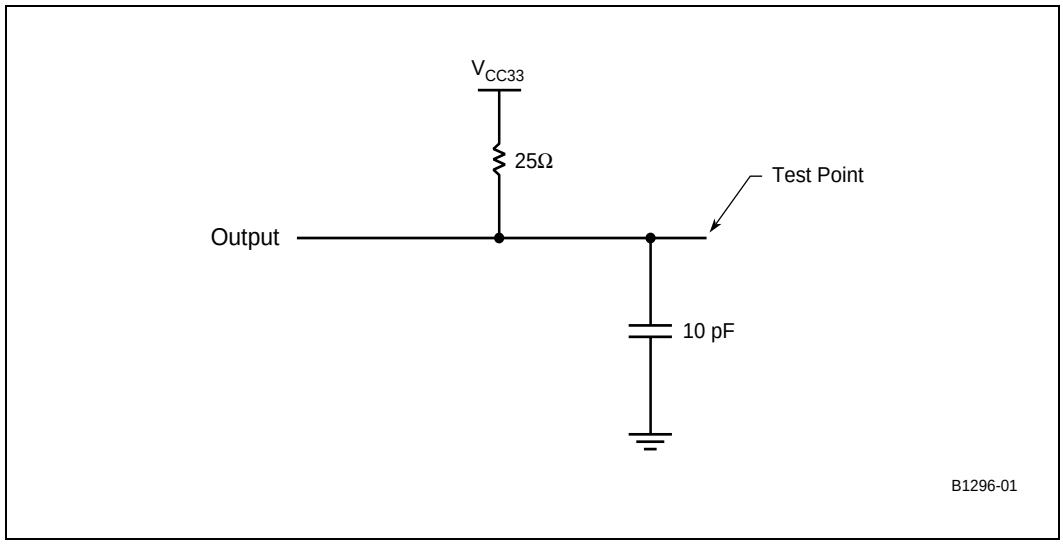
**Figure 10. PCI/PCI-X Tov(max) Rising Edge AC Test Load**



### 3.10.3 PCI/PCI-X $T_{ov(max)}$ Falling Edge AC Test Load

Figure 11 illustrates the PCI/PCI-X $T_{ov(max)}$ Falling Edge AC test load.

**Figure 11. PCI/PCI-X Tov(max) Falling Edge AC Test Load**




### 3.10.4 PCI/PCI-X $T_{ov(min)}$ AC Test Load

Figure 12 illustrates the PCI/PCI-X $T_{ov(min)}$ test load.

**Figure 12. PCI/PCI-X Tov(min) AC Test Load**